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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,308	09/23/2003	Bin Wan	REAP0495USA	3921

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NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
AHMED, ENAM	

ART UNIT	PAPER NUMBER
2112	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com.tw

Office Action Summary	Application No.	Applicant(s)	
	10/669,308	WAN ET AL.	
	Examiner	Art Unit	
	ENAM AHMED	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21 and 23-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21 and 23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Non – Final

This action is in response to applicants RCE filed on 3/22/08.

Response to amendment

The applicants arguments have been fully considered, and are only found persuasive to the extent that new reference Wulf et al. (U.S. Patent No. 6,154,826) in combination with Delvaux et al. (U.S. Patent No. 6,971,057) teaches for comparing the size of the cache memory with a product of the data length, N and an desired interleaving/de-interleaving depth, D to produce a control signal (column 3, lines 39-62), (column 6, line 50 – column 7, line 11), (column 7, lines 47-58), (column 8, lines 24-30), (column 9, lines 19-27), (column 9, lines 42-52), (column 10, lines 16-41), (column 14, line 66 – column 15, line 9), (column 20, lines 13-32) and (column 22, lines 42-48).

Response to applicants remarks

On page 10, the applicant states claim 1 patently defines over the prior art of record for at least the reason that the prior art of record fails to disclose the features emphasized above.

The Examiner agrees with the statement, however would like to point out new reference Wulf et al. (U.S. Patent No. 6,154,826) in combination with Delvaux et al. (U.S. Patent No. 6,971,057) teaches comparing the size of the cache memory with a product of the data length, N and an desired interleaving/de-interleaving depth, D to produce a control signal (column 3, lines 39-62), (column 6, line 50 – column 7, line 11), (column 7, lines 47-58), (column 8, lines 24-30), (column 9, lines 19-27), (column 9, lines 42-52), (column 10, lines 16-41), (column 14, line 66 – column 15, line 9), (column 20, lines 13-32) and (column 22, lines 42-48).

35 U.S.C. 103 Rejection

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having

ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 21 and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Delvaux et al. (U.S. Patent No. 6,971,057) in view of Wulf et al. (U.S. Patent No. 6,154,826).

With respect to claims 1 and 12, the Delvaux et al. reference teaches a main memory for storing a plurality of bytes, each at a separate address (column 3, lines 21-37); a cache memory for storing a plurality of bytes, each at a separate address, wherein the size of the main memory is larger than that of the cache memory (column 10, line 56 – column 11, line 27) and (column 3, lines 11-37); writing bytes of each first word into either the main memory or the cache memory (column 12, lines 34-51); for transferring bytes between the main memory and the cache memory according to the control signal (column 11, lines 15-21); for reading bytes out of the cache memory or the main memory and forming each second word there from according to the control signal such that each second word comprises bytes of more than one of the first words (column 12, line 52 – column 13, line 11), (column 21, lines 1-29). The Delvaux et al. reference does not teach coupled to the main memory and the cache memory, for comparing the size of the cache memory with a product of the data length, N and an desired interleaving/de-interleaving depth, D to produce a control signal. The Wulf et al. reference teaches coupled to the main memory and the cache memory, for comparing the size of the cache memory with a product of the data length, N and an desired interleaving/de-interleaving depth, D to produce a control signal (column 3, lines 39-62), (column 6, line 50 – column 7, line 11), (column 7, lines 47-58), (column 8, lines 24-30), (column 9, lines 19-27), (column 9, lines 42-52), (column 10,

lines 16-41), (column 14, line 66 – column 15, line 9), (column 20, lines 13-32) and (column 22, lines 42-48). Thus, it would have been obvious to one ordinary skill in the art at the time of the invention was made to have combined the references Delvaux et al. and Wulf et al. to incorporate coupled to the main memory and the cache memory, for comparing the size of the cache memory with a product of the data length, N and an desired interleaving/de-interleaving depth, D to produce a control signal into the claimed invention. The motivation for coupled to the main memory and the cache memory, for comparing the size of the cache memory with a product of the data length, N and an desired interleaving/de-interleaving depth, D to produce a control signal is because to get the best performance out of such a system, advantage must be taken of the architecture's available concurrency (column 2, lines 49-51 - Wulf et al. reference).

With respect to claim 2, the Delvaux et al. reference teaches wherein the cache memory And the control circuit are implemented within a single integrated circuit (see Fig. 6), (column 11, line 66 – column 12, line 12); and wherein the main memory is external to the IC (column 12, lines 27-330.

With respect to claim 3, the Delvaux et al. reference teaches wherein the control circuit operates in a burst read mode in which it reads bytes stored at a plurality of sequential addresses of the main memory whenever it read accesses the main memory (column 1, lines 17-22), (column 2, lines 18-40), and column 2, line 41 – column 3, line 7); wherein the control circuit operates in a burst mode in which it writes bytes to a plurality of sequential adresses of the main memory whenever it write accesses the main memory (column 1, lines 17-220, (column 2, lines 18-40) and column 2, line 41 – column 3, line 7); wherein the control circuit independently read and write accesses each individual addrress of the cache

memory whenever it reads a byte from or writes a byte to the cache memory (column 11, lines 28-55).

With respect to claim 4, the Delvaux et al. reference teaches wherein the control circuit writes bytes of each first word into the main memory so they are addressed in the main memory in an order in which those bytes appear in the first word (column 12, lines 34 – 40); wherein the control circuit reads bytes out of the main memory and writes them to the cache memory (column 12, lines 40-51); wherein the memory control circuit forms each second word from bytes it reads out of the cache memory (column 14, lines 24 – 46).

With respect to claim 5, the Delvaux et al. reference teaches wherein the control circuit writes bytes of each first word into the cache memory (column 13, lines 6-11); wherein the control circuit reads bytes of the first words out of the cache memory and writes them to the main memory such that they are addressed in the main memory in an order in which they are to appear in the second words (column 14, lines 34-46); and wherein the control circuit forms each second word from bytes it reads out of the cache memory and the main memory (column 11, lines 28-30), (column 14, lines 24-46).

With respect to claim 6, the Delvaux et al. reference teaches an input buffer for receiving and storing bytes forming each first word (column 17, lines 50-55); wherein the control circuit reads bytes forming each first word from the input buffer (column 11, lines 37- 41); and writes them to the main memory so that they are addressed in the main memory in an order in which the bytes appear in that first word (column 12, lines 34-51); and also reads bytes

forming first words out of the input buffer and writes them to the cache memory (column 11, lines 51-55); and an output buffer, wherein the control circuit forms the second words in the output buffer by reading bytes out of the cache memory and writing them into the output buffer (column 11, lines 28-55).

With respect to claim 7, the Delvaux et al. reference teaches an input buffer for receiving and storing each first word (column 17, lines 50-55), wherein the control circuit transfers bytes forming each first word from the input buffer to the cache memory (column 11, lines 51-55); an output buffer, wherein the control circuit forms the second words in the output buffer by reading bytes out of the main memory and out of the cache memory and writing them into the output buffer (column 11, lines 28-55).

With respect to claim 8, the Delvaux et al. reference teaches wherein the control circuit writes every byte of each first word into the main memory (column 11, lines 37-55), (column 14, lines 7-16).

With respect to claim 9, the Delvaux et al. reference teaches wherein the control circuit writes some, but less than all, bytes of each first word into the main memory (column 8, lines 41-63).

With respect to claim 10, the Devlaux et al. reference teaches wherein the control circuit writes every byte of each first word into the main memory (column 11, lines 37-55), 9column 14, lines 7-16).

With respect to claim 11, the Delvaux et al. reference teaches wherein the control circuit writes some, but less than all, bytes of each first word into the main memory (column 8, lines 41-63).

With respect to claim 13, the Devlaux et al. reference teaches wherein a plurality of bytes are read from a plurality of sequential addresses of the main memory in a burst read mode of accessing the main memory whenever the main memory is read accessed (column 1, lines 17-22), (column 2, lines 18-40), and column 2, line 41 – column 3, line 7); wherein the plurality of bytes are written to a plurality of sequential addresses of the main memory in a burst mode whenever the main memory is write accessed column 1, lines 17-220, (column 2, lines 18-40) and column 2, line 41 – column 3, line 7); wherein a single address of the cache memory is independently read or write accessed whenever the cache memory is read or write accessed (column 11, lines 28-55).

With respect to claim 14, the Devlaux et al. reference teaches wherein the step of writing bytes of each first word into the main memory so that they are addressed in the main memory in an order in which those bytes appear in that first word (column 12, lines 34-51); wherein the step of transferring comprises reading bytes out of the main memory and writing them to the cache memory (column 11, lines 51-55); wherein he step of reading comprises

forming each second word from bytes read out of the cache memory (column 11, lines 28-55)..

With respect to claim 15, the Delvaux et al. reference teaches wherein the step of writing comprises writing bytes of each first word into the cache memory (column 13, lines 6-11); wherein the step of transferring comprises reading bytes out of the cache memory and writing them to the main memory (column 14, lines 34-46); and wherein thhe step of reading comprises forming each second word from bytes read out of the cache memory and the main memory (column 11, lines 28-30), (column 14, lines 24-46).

With respect to claim 16, the Delvaux et al. reference teaches storing bytes forming each first word in an input buffer (column 17, lines 50-55); reading bytes of each first word stored in the input buffer and writing them to the main memory (column 11, lines 41-55); reading selected bytes of each first word stored in the input buffer and writing them to selected addresses of the cache memory (column 12, lines 34-51); wherein the step of transferring comprises reading bytes out of the main memory and writing them into a cache memory (column 11, lines 51-55); wherein the step of writing comprises reading bytes forming the second word out of the cache memory and writing them into an output buffer (column 11, lines 28-55).

With respect to claim 17, the Delvaux et al. reference teaches storing bytes forming the first word in an input buffer (column 17, lines 50-55); reading bytes of the first word from the input buffer and writing them to the cache memory (column 11, lines 51-55); wherein the

step of transferring comprises reading bytes forming the first word out of the cache memory and writing them to the main memory (column 14, lines 34-46); reading bytes forming the second word out of the main memory and out of the cache memory (column 11, lines 28-30), (column 14, lines 24-46); and writing them into an output buffer to form the second word in the output buffer (column 11, lines 28-55).

With respect to claim 18, the Delvaux et al. reference teaches reading bytes of the step of writing comprises reading all bytes of the first word out of the input buffer and writing them into the main memory (column 11, lines 37-55), (column 14, lines 7-16).

With respect to claim 19, the Delvaux et al. reference teaches reading less than all bytes of the first word out of the input buffer and writing them to the main memory (column 8, lines 41-63).

With respect to claim 20, the Delvaux et al. reference teaches reading all bytes of the first word written into the cache memory back out of the cache memory and writing them to the main memory (column 14, lines 34-46).

With respect to claim 21, the Delvaux et al. reference teaches reading less than all of the bytes of the first word written into the cache memory back out of the cache memory and writing them into the output bufer (column 11, lines 28-55).

With respect to claims 23 and 25, the Delvaux et al. reference teaches wherein the size of the cache memory is not smaller than a product of a maximum of the interleaving/de-interleaving depth and a number of bytes read from or written to sequential addresses of the main memory during each read or write access (column 3, lines 11-37).

With respect to claims 24 and 26, the Delvaux et al. reference teaches wherein the size of the main memory is not 20 smaller than a product of a largest allowable interleaving/de-interleaving depth and a largest allowable byte width of code word (column 3, lines 11-37).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Enam Ahmed whose telephone number is 571-270-01729. The examiner can normally be reached on Mon-Fri from 8:30 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Louis Jacques Jacques, can be reached on 571-272-6962.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EA

5/15/08

/JACQUES H LOUIS-JACQUES/

Supervisory Patent Examiner, Art Unit 2112